Electronic Version
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Claims

[c1] A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor on a semiconductor wafer, the method comprising:
creating a first spacer and a second spacer on the n-type field effect transistor and on the p-type field effect transistor;
removing at least a portion of the first spacer on the p-type field effect transistor; and
depositing silicide forming material on the silicon wafer, such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor and compressive mechanical stresses are formed within a channel of the p-type field effect transistor.

[c2] The method of claim 1, wherein the step of removing comprises etching at least a portion of the first spacer of the p-type field effect transistor to form a gap beneath the second spacer, the portion of the first spacer being located under the second spacer of the p-type field effect transistor.

[c3] The method of claim 2, wherein the step of depositing silicide material comprises depositing silicide material on the n-type field effect transistor and on the p-type field effect transistor such that the silicide material fills at least a portion of the gap of the p-type field effect transistor and the silicide material is closer to a gate edge of the p-type field effect transistor than a gate edge of the n-type field effect transistor.

[c4] The method of claim 1, wherein the step of creating a first spacer and a second spacer comprises:
creating an oxide spacer on the n-type field effect transistor and on the p-type field effect transistor; and
creating a nitride spacer on the n-type field effect transistor and on the p-type field effect transistor.

[c5] The method of claim 4, wherein the step of creating oxide spacers comprises:
depositing oxide on the silicon wafer; and
etching a portion of the deposited oxide to form the oxide spacer.

[c6] The method of claim 5, wherein the step of creating nitride spacers comprises:
depositing nitride on the silicon wafer; and
etching a portion of the deposited nitride to form the ni-

tride spacer, wherein the nitride spacer sits on the oxide spacer.

[c7] The method of claim 1, wherein tensile stresses between about 500MPa and 3GPa are formed in the channel of the n-type field effect transistor.

[c8] The method of claim 1, wherein compressive stresses between about 500MPa and about 3GPa are formed in the channel of the p-type field effect transistor.

[c9] The method of claim 1, further comprising removing silicide material from above the n-type field effect transistor and the p-type field effect transistor.

[c10] The method of claim 1, wherein the step of depositing silicide material comprises depositing at least one of Co, HF, Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr.

[c11] The method of claim 1, further comprising removing the mask used to cover the n-type field effect transistor.

[c12] A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor on a semiconductor wafer, the method comprising the steps of:
creating a spacer having a first width for the n-type field

effect transistor and creating a spacer having a second width for the p-type field effect transistor, the first width being greater than the second width; and
depositing silicide forming material on the semiconductor wafer such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor and compressive stresses are formed within a channel of the p-type field effect transistor.

[c13] The method of claim 12, wherein the creating step comprises the step of
etching at least about a 20nm to about a 50nm portion of an oxide spacer of the p-type field effect transistor.

[c14] The method of claim 12, wherein the creating step comprises the step of
etching at least about a 20nm to about a 50nm portion of an oxide spacer of the p-type field effect transistor.

[c15] The method of claim 12, wherein the silicide material is deposited closer to a gate edge of the p-type field effect transistor than a gate edge of the n-type field effect transistor.

[c16] The method of claim 12, wherein the creating step comprises the steps of:
depositing a first material on the silicon wafer;

etching at least a portion of the deposited first material to form a first spacer;
depositing a second material on the silicon wafer;
etching at least a portion of the deposited second material to form a second spacer, wherein at least a portion of the second spacer is formed on the first spacer.

[c17] The method of claim 16, wherein the first material is oxide.

[c18] The method of claim 17, wherein the second material is nitride.

[c19] The method of claim 16, further comprising etching at least a portion of the deposited first material located under the second spacer.

[c20] The method of claim 12, wherein tensile stresses between about 500M Pa and 3G Pa are formed in the channel of the n-type field effect transistor.

[c21] The method of claim 12, wherein tensile stresses between about 500M Pa and 3G Pa are formed in the channel of the n-type field effect transistor.

[c22] The method of claim 12, wherein the width of the spacer having the first width is about 20nm to about 50nm less than the width of the second spacer having the second

width.

[c23] The method of claim 12, wherein the width of the spacer having the second width is between about 20nm and about 100nm.